



QScan

QT900 – Boundary Scan Test System



IEEE 1149.1 compliant JTAG port

Boundary Scan Controlled Synchronous Digital I/O channels

End-to-end Functional test

Individually configurable bi-directional I/O channels

Programmable voltage levels for Digital I/O

Specific set of channels can be bypassed to minimize scan time.

Optional : Boundary Scan Controlled Synchronous Analog I/O

New generation densely populated, multi-layered boards (PCBs) mounted with boundary scan compliance devices, along with non-boundary scan digital and mixed signal devices toss a real challenge when comes for testing and or trouble-shooting.

QScan offers a unique solution in testing these kinds of boards with its easy to use software and libraries. It can perform various tests including interconnect test between JTAG devices and edge connector, functional tests for non boundary scan devices using Boundary Scan Devices' I/O pins (Virtual test points) and digital I/O channels.

Use of virtual test pins and edge connector eliminates the need for expensive test fixture strategy using bed of nails or using a limited channel-flying probe.



Boundary Scan Interconnect with Card Edge



A Test Pass Screen in Boundary Scan Interconnect

TEST METHODOLOGY

The QScan Test System is designed to provide test solution for both Boundary Scan Compliance Devices and Non-Boundary Scan Devices. The system provided with Digital I/O channels capable to drive and receive via JTAG IEEE 1149.1 interface and synchronous to JTAG pins. Both the Digital and JTAG tests are carried out synchronously. Even if the board under test does not have any JTAG devices, still the system's Digital and Analog I/O can be used for functional test of the board using edge connectors.

The QScan provides maximum of 320 Digital bi-directional test channels with 2 mega bits one shot drive and capture RAM. Each channel can be individually configured as an input or output. During testing, the programming and controlling of the test channels are automatically performed by system software.

Using the waveform editor the user can generate non-boundary scan device functionality test patterns. The digital I/O and virtual test channels' mapping can be provided by fixture mapping tool.

The digital I/O cards have 64 channels grouped in to 4 banks. Each bank's channel voltage levels can be programmed using pallet setting option in the software. The 4 pallets are selectable in the range of 1.8V, 2.5V, 3.3V and user programmable.

Guided Probe back tracking is available for detection of the origin of the fault during a board functional test, when net-list is entered in the system software.

Microsoft Internet Explorer

Tuesday, October 30, 2007

Stuck at zero nets

| Net Name | Nodes | Remarks |
|----------|-------|---------|
| Net_27 | U2_32 | |
| Net_29 | U2_33 | |
| Net_30 | U2_72 | |

Stuck at non nets

| Net Name | Nodes | Remarks |
|----------|--------|---------|
| Net_31 | U5_155 | |
| Net_32 | U5_56 | |
| Net_33 | U2_B3 | |
| OABT7 | U4_36 | |

Shorted Nets

| Net Name | Nodes | Remarks |
|----------|-------------|---------|
| ACT8 | U3_15,U4_12 | |
| ACT2 | U3_22,U4_3 | |
| ACT3 | U3_21,U4_5 | |
| ACT4 | U3_20,U4_6 | |
| ACT5 | U3_19,U4_8 | |
| ACT6 | U3_17,U4_9 | |

Details of Learnt Nets

Qmax TestDirector 6 Test Sequencer

Test Name: EDGE_FUNCTIONAL_TEST Description:

Signal List:

| Signal | Signal Connection Type | Signal Nodes | Edge Mode | Change I/O |
|------------|------------------------|--------------|-----------|------------|
| ACT5 | Edge Connector | U2_B | JT2_1 | Output |
| LATCHOUT8 | | | | |
| LATCHOUT17 | | | | |
| LATCHOUT2 | | | | |
| LATCHOUT3 | | | | |
| LATCHOUT4 | | | | |
| LATCHOUT5 | | | | |
| LATCHOUT7 | | | | |
| BUOE2 | | | | |
| BUOE1 | | | | |
| GMW2 | | | | |
| ACTOP2 | | | | |
| ABTOLDB | | | | |

List of Card edges and Details:

| S No | Signal Name | Edge Name | Edge Type | Palette | Channel |
|------|-------------|-----------|-----------|----------|---------|
| 2 | FDI1 | U2_B10 | BiSide | | |
| 3 | CLK1 | U2_C12 | BiSide | | |
| 4 | PR1 | U2_A12 | BiSide | | |
| 5 | D1 | U2_45 | BiSide | | |
| 6 | GMW1 | U2_46 | BiSide | | |
| 7 | D2 | U2_44 | BiSide | | |
| 8 | PR2 | U2_C3 | BiSide | | |
| 9 | CLK2 | U2_A10 | BiSide | | |
| 10 | CLK2 | U2_D8 | BiSide | | |
| 11 | FDI2 | U2_B9 | BiSide | | |
| 12 | GMW2 | JT2_1 | Output | Palette0 | 0 |

Boundary Scan – Card Edge Studio – Main Window

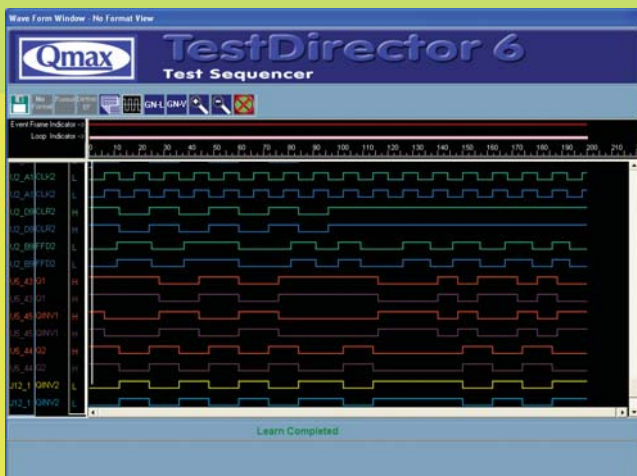
Select the Boundary scan devices

Check for Boundary scan devices available in this board : Detect scan path

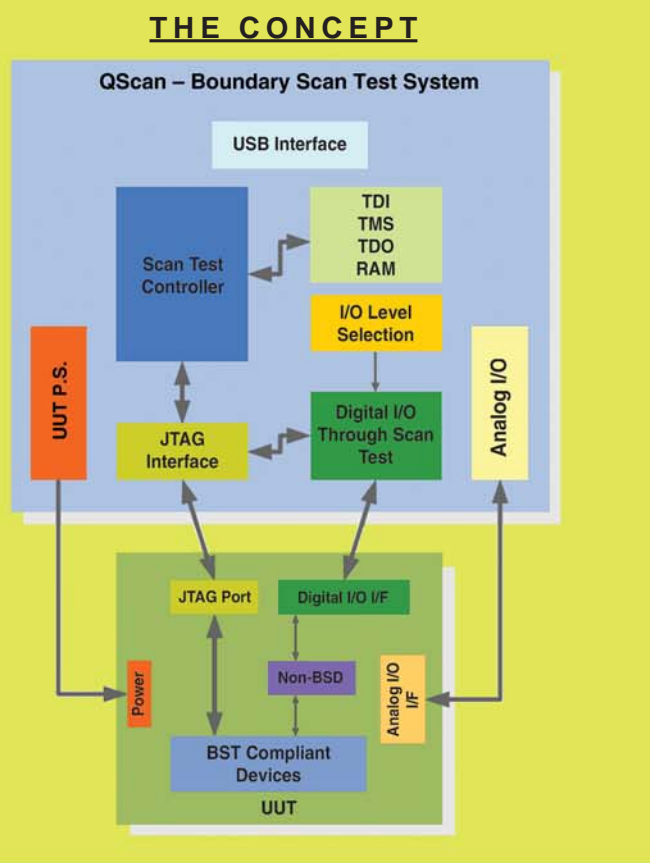
List of boundary scan devices available in this board :

| Location | Device Name | Package | Idcode | Usercode |
|----------|-----------------|---------|----------|----------|
| U1 | XC18V04_PC44_V2 | PC44 | F5036093 | ... |
| U2 | XC2V40_FG256 | FG256 | 21008093 | ... |
| U3 | SN74BCT8244A | DW | BYPASS | ... |
| U4 | SN74ABT18245A | DL | 1000502F | ... |
| U5 | XC95216_160PQ | PQ_160 | 29512093 | ... |

Boundary Scan Detection



Waveform Window



FEATURES

Scan chain detection

User code / Device code verification

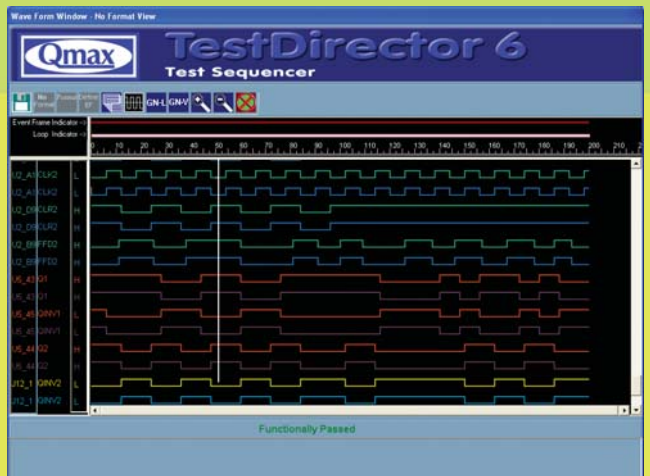
Boundary Scan Interconnect test.

Board Functional Test

Functional testing of ICs in out-circuit condition using external IC sockets and adapters with Qmax's Library option.

Digital I/O channels are 5V tolerant and the voltage levels are programmable from 1.8V to 3.3V in groups of 16 channels.

Each set of 32 I/O channels can be bypassed to save scan time for UUTs, which require less than 320 I/O channels.



Waveform Window with Pass message



Boundary Scan Test done on a Radar Controller PCB

SPECIFICATIONS

JTAG PORT

Auto Sense and switches to 1.8V, 2.5V, 3.3V and 5V

TCK frequency Maximum 25MHz — Programmable

I/O CHANNELS

Digital I/O from minimum of 64 to maximum of 320 in steps of 64 channels.

Programmable I/O Levels 1.8V to 3.3V

Channels : 5V tolerant, for 3.3V Drive.

Optional Anlaog I/O minimum of 2 drive / sense channels and maximum of 4

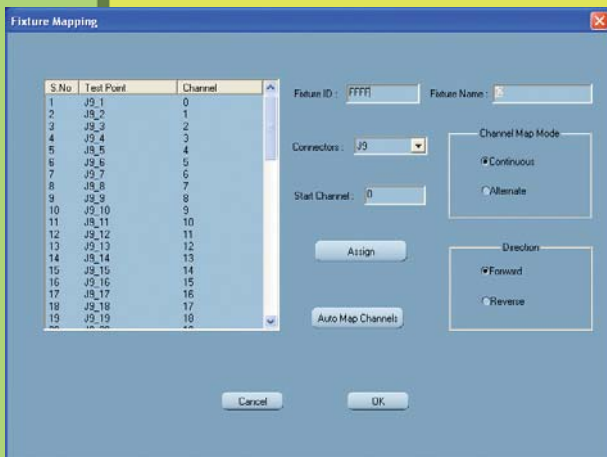
Unit Under Test (UUT) Power Supply 3.3V @ 12A

+5V @ 22A

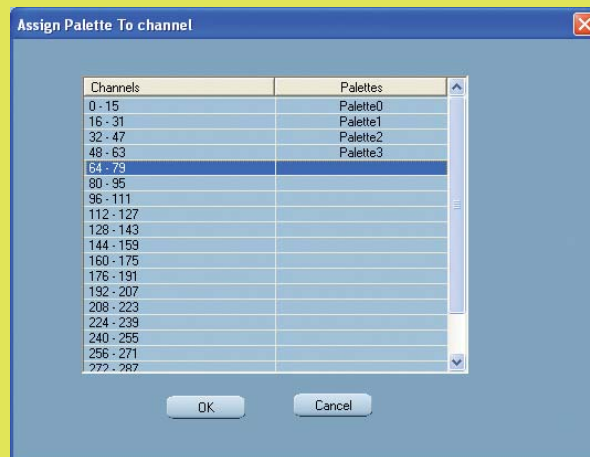
-5V @ 0.5A

+12V @ 10A

-12V @ 0.5A



Fixture Defenition



Palette Setting



Testing of ICs in Out-Circuit mode using Qmax's QScan - Boundary Scan Test System



— where standards are set; not matched.

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