Qmax

V250

Advanced Desk-Top ATE

In-Circuit Functional Test

QSM VI Learn & Compare

R, L, C, V, F Measurements

Board Functional Test & Guided Probe Back Track

Integrated Boundary Scan Test with Edge Pins

PXI Instrumentation Ready

V250 is a cost effective ATE system, designed to cater the needs of PCB test and repair depots, keeping in mind the changing PCB technology and the challenges in testing them off-line. It can provide complete PCB test and diagnostic functions for any kind of PCB including the latest very high density complex PCBs with high pin count PQFP, FPGA VLSI chips.

V250 is a Combinational Mixed Signal Test System with the addition of Boundary Scan Test for the latest generation boards. It has Card Edge Functional Test for both digital and analog, and In-Circuit Functional Test for localized test of individual devices with a large Library support and using VHDL simulator. It also incorporates an advanced QSM VI with user definable wave pattern.

V250 is designed to interface to the UUT through simple clips and probes or through card edge or through a bed of nail test fixture for up to 256 test pins. In addition, it has the Boundary Scan Test option for virtual pin test where the number of virtual test pins has no physical limit.

It's basic timing unit is 40ns and thus can generate test patterns at 25 MHz data rate. It has 256K x 8 RAM behind each digital pin and 256K x 28 RAM behind every analog channel. Its advanced sequencer allows external event synchronization or handshake, which are very essential in complex micro-processor tests.

# TestDirector-6 — An Innovative Test Software

In-Circuit Functional Test at its Best

✿ Functional Test facility for testing individual ICs in In-Circuit or Out-of-Circuit.
✿ Pin Status Check & In-built DRC (Design Rule Checker).
✿ IEEE Standard VHDL or QDDL (Qmax device Description Language) language in behavioral description of the function of the chip in its library.
✿ PythonTD Test language for Analog / Mixed signal device stimulus and output evaluation.
✿ Auto compensation is extended for all digital devices (not limiting to SSI /MSI) and thus LSI / VLSI chips can be tested in its In-Circuit configuration without the need to learn from a known good board.
✿ On-Line Instant simulation helps testing devices in any In-circuit condition such as reset pin disabled counters or LSI devices in various configurations and in-circuit links.
✿ Identify Unknown or House codes devices including LSI devices.
✿ Unified Library of 31K+ devices and device test comprehensives report for validation of Library Test programs developed by a user.
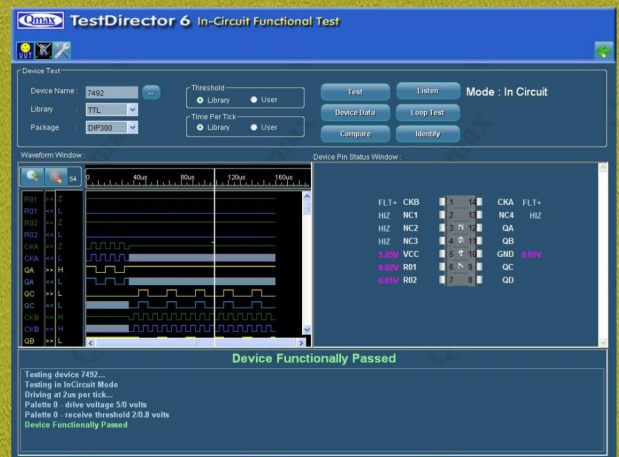
User Defined QSM VI Stimulus

✿ User defined wave pattern as stimulus for VI Trace and thus not limiting the VI trace to simple sine wave alone.
✿ User defined wave pattern can be any mathematical wave shape such as sine / triangle /square /step /ramp or even arbitrary patterns as desired by user and can be stored in the Library for possible re-use.
✿ The frequency is fully programmable from as fast as 100 KHz down to 1 Hz as a result of V250's vast time base selection capability.
✿ Programmable amplitude, source impedance.
✿ Use of Step wave is useful in analyzing transient response of node.
✿ Frequency Sweep generation for frequency response of a node.
✿ Incorporates interactive mode as well as learn and compare.
✿ Fixed Reference, any pin to any pin or user combination.
✿ DRC check before power on in QSM VI tests using its vast library.
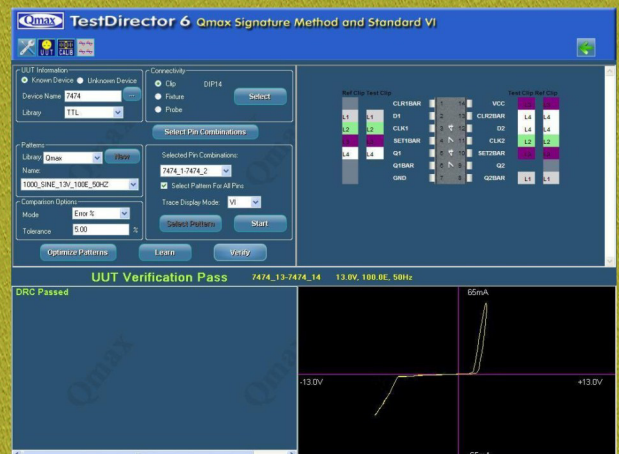
Measurement Functions & Other Utilities

✿ Resistance / Inductance / Capacitance / Voltage Measurements.
✿ Diode Measurements.
✿ Frequency Measurement.
✿ Period /Time Measurements.
✿ 4 Channel - 10 Mega Sample Scope with Programmable Load.
✿ 4 Channel Function Generator

TD6 TestSequencer

✿ For Sequencing of multiple tests with conditional branching, messaging, user prompting, external trigger and external handshake.
✿ Graphical User Interface for Adding Tests, Learn / Compare, Stability Check with clear colour code on the Board Layout JPEG image.
✿ Board level test using combination of isolated device test (ICFT), QSM VI, Measurements, Card Edge Functional Test, Integrated Card Edge + Boundary Scan Test*, all in one test program.
✿ Automatic Guarding Guide for Tri-State / OC / OE devices.
✿ Automatic update of device links in the Net-List.
✿ Compare Net-List with device links feature.

Card Edge Functional Test at its Best

✿ Integrated Card edge Test with Boundary Scan Virtual pins and Physical Test pins.
✿ User can develop test program for complex boards with ASICs and BGAs, where no functional data are available.
✿ User can generate the test vectors using the graphical waveform editor or PythonTD test vector generator, where the primary I/O pins can be either physical edge pin / In-Circuit pin or a JTAG Virtual Boundary Scan Pin.
✿ User can either learn from a known good board for expected output response or define the expected using either graphical waveform editor or the PythonTD test language with mask / tolerance editing facilities or use the simulated output response.
✿ Graphical waveform editor and PythonTD supports Digital / Analog and Mixed Signal I/Os.
✿ The Test program developed can be used for a device /cluster or a complete PCB.
✿ In case of cluster or whole board, user needs to input the netlist of the circuit, assign input /output pins for tester channel for automatic generation of guided probe back tracking of internal nodes.
   * *Boundary Scan Software need to be purchased for enabling this facility.*

Boundary Scan Test Software (Optional)

✿ Boundary Scan uses simple 5-wire connector (J-TAG) to interface to the PCB under test, eliminating the need for test pin contact (Virtual Test Pin Test Concept).
✿ Using Boundary Scan Software package and vendor supplied BSD Files, ID Code Read, User Code Read, Integrity Test and Interconnect Test can be performed.
✿ Learn and compare option for interconnect test, where no netlist is available.
✿ Functional Test for BS devices and Non-Boundary Scan Devices (Glue Logic Chips).
✿ Integrated Card Edge and Boundary Scan Test for Interconnect Test and Board Functional Test.

TD6 TestStation

✿ Programs developed in TestDirector 6 TestSequencer can be exported to TestStation
✿ Test only function and no program /data /tolerance can be modified.
✿ For operator use only.
✿ User defined Error Log reporting, Failure analysis, statistics and data log.
✿ Optional Remote Monitoring of yield and statistics.

TD6 IDTE (Optional)

✿ For developing new Digital Device Models in the library using VHDL / QDDL functional behavior.
✿ For developing new Analog / Mixed signal device models using PythonTD Test Language and adding it in the Library.
✿ Graphical Test Program Generation feature

TD6 TestSim Suite (Optional)

✿ For Board Level VHDL model creation and functional simulation of the board using VHDL. Advanced On-Line Simulation support for increased fault coverage for boards that fail to initialize.
✿ Automatic Guided Probe Back Tracking for Fault Isolation up to node level.
✿ Fault Simulation Software for Board Test Program validation and test comprehensiveness.
✿ Fault Dictionary Software for nil or minimized internal node probing.

TD6 CircuitTracer (Optional)

✿ Using multiple clips, Edge connectors / Probes and JTAG IO pins, the connectivity between devices can be learnt and a netlist created.
✿ Created net list can be imported into optional Edwin CAD package for schematic generation.

S P E C I F I C A T I O N S

SYSTEM

Test Channels	Basic 64 expandable up to 256 (32 Ch. per card)
	Un-limited Virtual Test Points (JTAG)
Pattern Rate	25 MHz -Digital testing (Max.),
	10 MHz -Analog testing,
	(25 MHz sampling rate)
	100 KHz QSM VI
Time Base	Programmable from 40ns to 167ms in steps of 10ns
Dynamic Guarding	Up to 8 dedicated channels, allocated automatically. Additionally, any digital channel can be used for Guarding applications.

DRIVERS / SENSORS

DIGITAL

Driver/Sensor card	32 ch. Bi-directional RAM based ch. per card up to 256 max
Drive Level & Resolution	±10V programmable in 10 mV steps
Sense Level & Resolution	±10V programmable in 10 mV steps
Current	650 mA sink & source limit
Driver state	Hi, Low and Tri-state

ANALOG

No. of Channels	Four, 14 bit DAC / ADC RAM based,
Analog Multiplexer	Switchable to any test channel available.
Driver output current	250mA per pin /ch.
Drive Pattern	User definable and standard waveform
Drive Source Impedance	Programmable in 8 steps
Drive current/voltage	± 250mA maximum / ±25 volt per Channel.

IN-CIRCUIT TEST

Digital	Clip on test using systems device library and simulator output.
	On-board clock disable H/W feature for In-Circuit testing
Analog	Clip on test using systems device library and simulator/calculated output.
Simulator	Industry grade VHDL simulator

OTHER FEATURES

Size of test	4K X 60 bits-deep test vectors in Single burst mode. Unlimited vector depth in interactive hand shake mode
Analog Measurement	R, L, C, V and F
	Res.: 10Ohms to 1MOhms Cap.: 200pF to 10000 μF Inductance: 100μH to 10H Voltage: +/–25V Frequency: Up to 48 MHz
	4 Channel Osclloscope with programmable load.
BUT Power Supply	+3.3V@10A / +5V@10A /–5V@10A / +15V@8A /–15V@8A. Optional : Programmable Power Supply (0–36V @ 6A) up to 2 Nos.
Dual Signature trace	Standard feature. Signature plotting through two probes or set of clips.

System General Specifications

Power Requirement	230V AC / 5A, 1200W, 50-60 Hz
Physical Dimension	560mm (w) X 540mm (d) X 310mm (h), Rittal, Ri Case 6U Cabinet
Weight	30 Kg (net)

TEST SOFTWARE

TD6 Interactive WorkStation	Standard.
TD6 TestSequencer	Standard.
TD6 TestStation	Standard
TD6 TestSim Suite	Optional
TD6 IDTE	Optional
TD6 CircuitTracer for Reverse engineering	Optional
Edwin for Windows XP for schematic generation	Optional
TD6 Boundary Scan Test	Optional

General *(Recommended)*

Controller	Pentium IV PC or higher
Operating System	Windows Vista Business or Ultimate
	Windows XP Professional Edition SP2
RAM	Minimum 2 GB
Hard Disk	80 GB with 2 partition
Interface	USB 2.0 (min. of 4 USB ports)
User Control	keyboard / Mouse / Optional Foot switch / external trigger.

TEST INTERFACE (Optional)

IN-CIRCUIT WALKING CLIPS

DIP Clips Top access	8-64 pins
DIP Clips Bottom	8-40 pins
PLCC Clips	up to 84 pins
SOIC Clips	up to 28 pins
QFP Clips	On request
TO5 package	
TO9 package	
Russian Device Clips	up to 40 pins
JTAG	5 wire connector for boundary scan tests.

OUT CIRCUIT

DIP 40 & 64

SMDs SOP / TSOP / PQFP / SOIC / SOJ / PLCC up to 64 pins

CUSTOMISED

Card edge / Bed of nails based test fixtures as per user applications.

Qmax

— where standards are set; not matched.

For more information mail to:
Sales@qmaxtest.com

or visit us at :
www.qmaxtest.com