Equip your students with leading edge technology

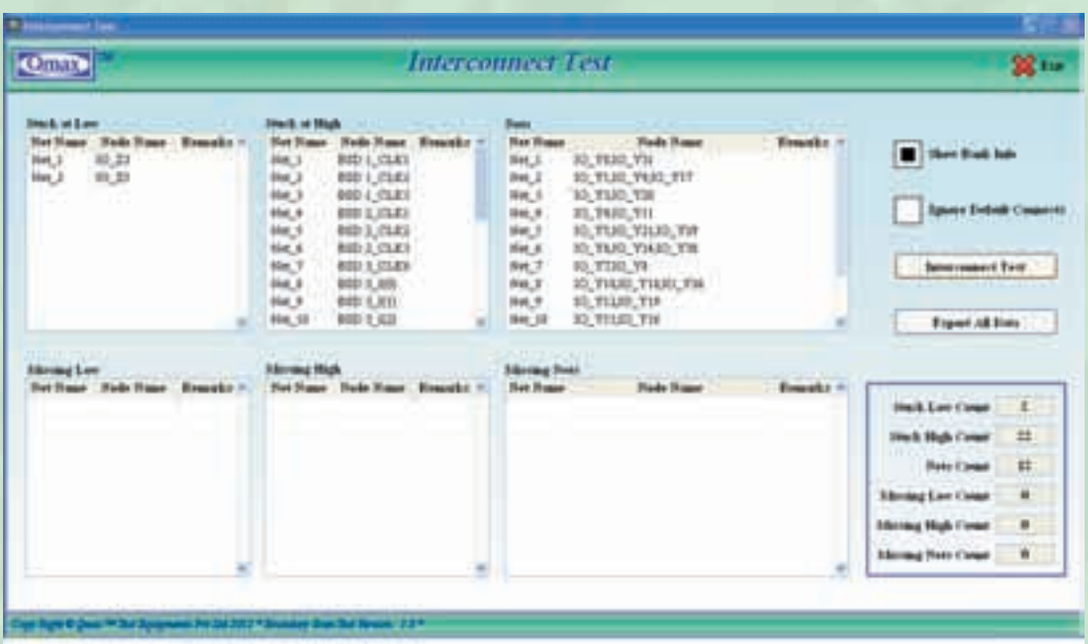
Qmax®

IEEE 1149.1 Boundary Scan Trainer Kit

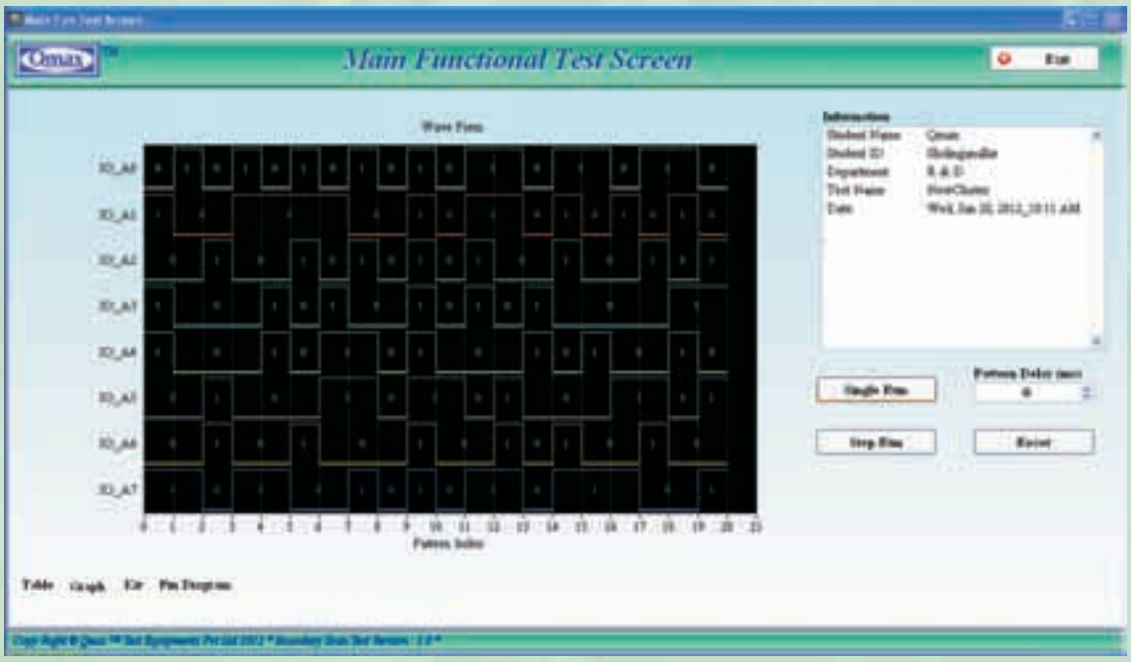
What is Boundary Scan?

Boundary Scan as defined by the IEEE STD 1149.1 is an integrated method for testing ICs and its interconnects on highly complex and dense printed circuit board with out using physical test probes. It is also widely used as a debugging method to analyze change in logic states within sub-blocks of IC.

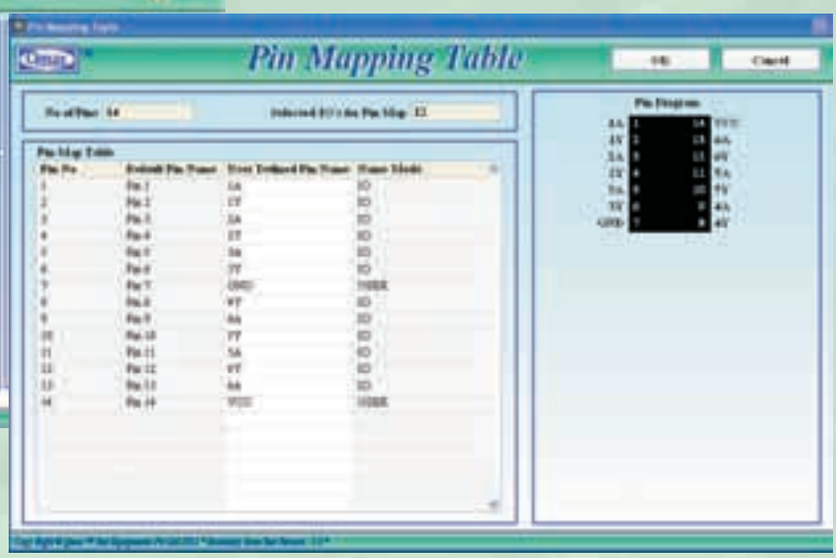
Scan Test performs a scan chain operation on a PCB to identify all the Boundary scan compatible devices available on board and the sequence in which they are connected to each other.



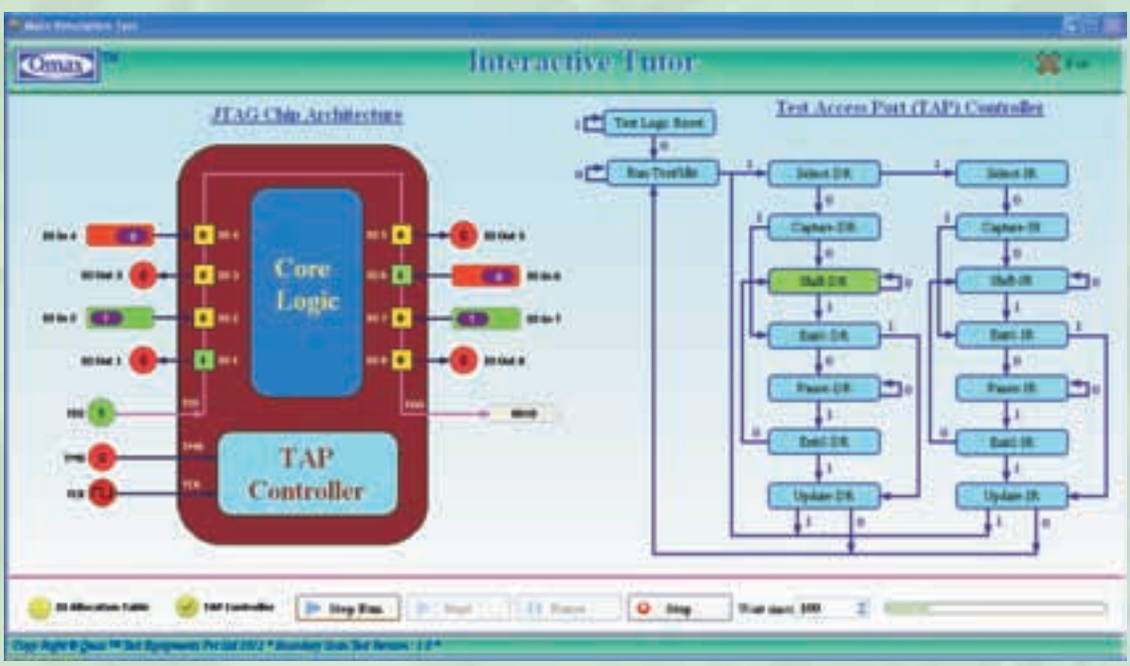
Interconnect test is like a board integrity check which checks for the interconnects that exist between various boundary scan device pins.



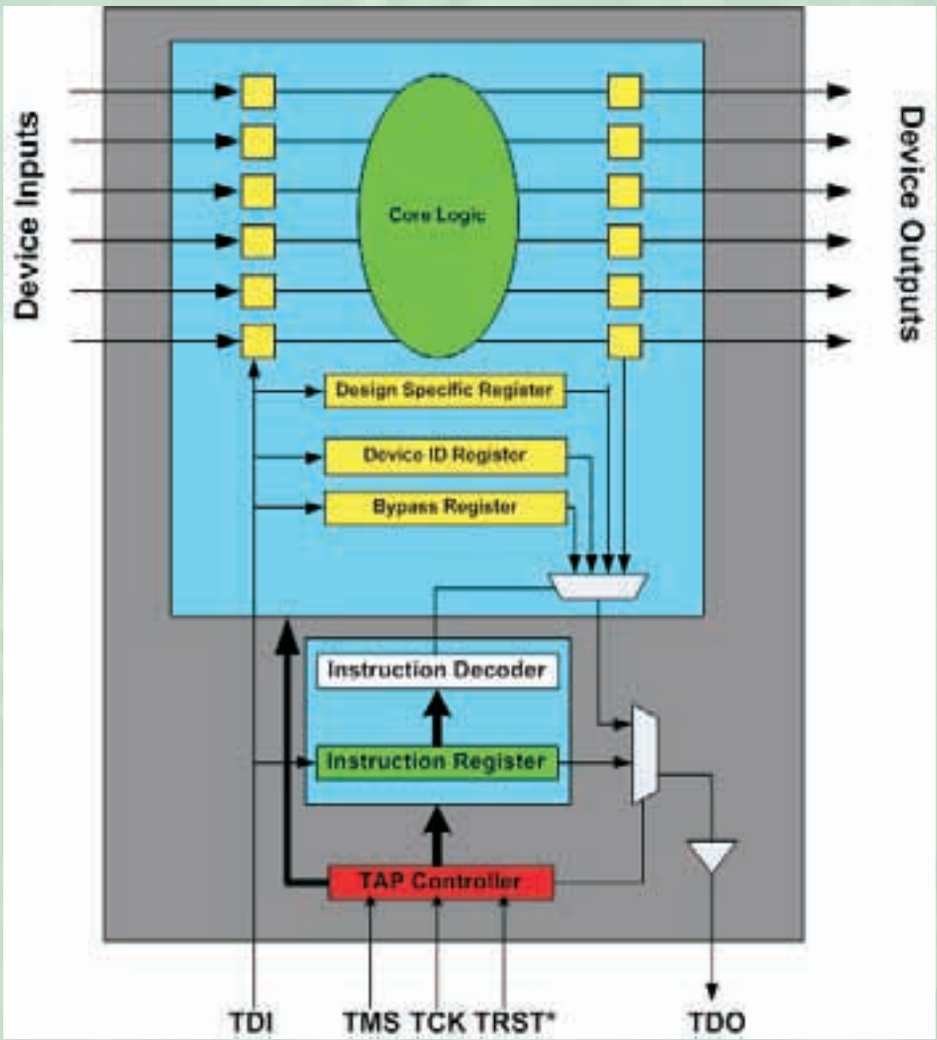
Functional truth table verification of various non-boundary scan digital devices on board using JTAG technology can be experimented.



Cluster Test allows user to develop various combinational circuits and verify its operation or function via JTAG 4 wire technique.



Interactive Tutor teaches users', the underlaying concept of Boundary scan and provides various simulations to strengthen their understanding.



Boudary Scan Architecture

The IEEE1149.1 Standard Boundary Scan Chip Architecture facilitates application to perform

- >> Chain Integrity Testing
- >> Interconnection Testing between devices
- >> Core logic Testing (BIST)
- >> In-system programming
- >> In-Circuit Emulation
- >> Functional Testing

Qmax Boundary Scan Trainer Kit is composed of a set of hardware module and software package with Tutorial and Hands-On-Labs that are meant to help user get familiar with the JTAG IEEE1149.1 Boundary Scan Standard for Testing BS compatible devices in an easy, interactive way. The USB2.0 interface makes it simple to install, connect and communicate to any PC.

Trainer KIT Contents

- >> JTAG Controller and Evaluation kit with USB Interface to PC
- >> Application Software Installation CD
- >> Teaching Tutorial on Boundary Scan
- >> Lab Experiments w/ Solutions
- >> Series of Hands on Exercises

Features

This Training Kit provides Hands-On-Labs that cover relevant concepts of JTAG Boundary Scan Testing IEEE STD 1149.1. The following labs are available:

Scan Test: Demonstrates how to perform scan test on BS compatible devices, how to bypass devices from scan chain

Interconnect Test: Demonstrates how to detect the interconnect between boundary scan devices and what various types of interconnects exist on a board

Functional Test: Demonstrates how to perform functional testing for Non Boundary Scan Digital devices using JTAG technology.

Cluster Test : Demonstrates how to test and trouble shoot a digital combinational logic using JTAG technology

Interactive Tutor: Provides user with an in depth understanding of the JTAG technology and the IEEE1149.1 standard principle of testing.

Each Lab includes:

A step-by-step document with code snippets and screen-shots that walks you through the key features.

An end solution for each exercise in the lab, with the resulting application after performing all the lab's steps.

A series of exercises to hands on and test your understanding of the JTAG Technology.

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— where standards are set; not matched.

For more information, mail to :
sales@qmaxtest.com
Or visit us at :
www.qmaxtest.com

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