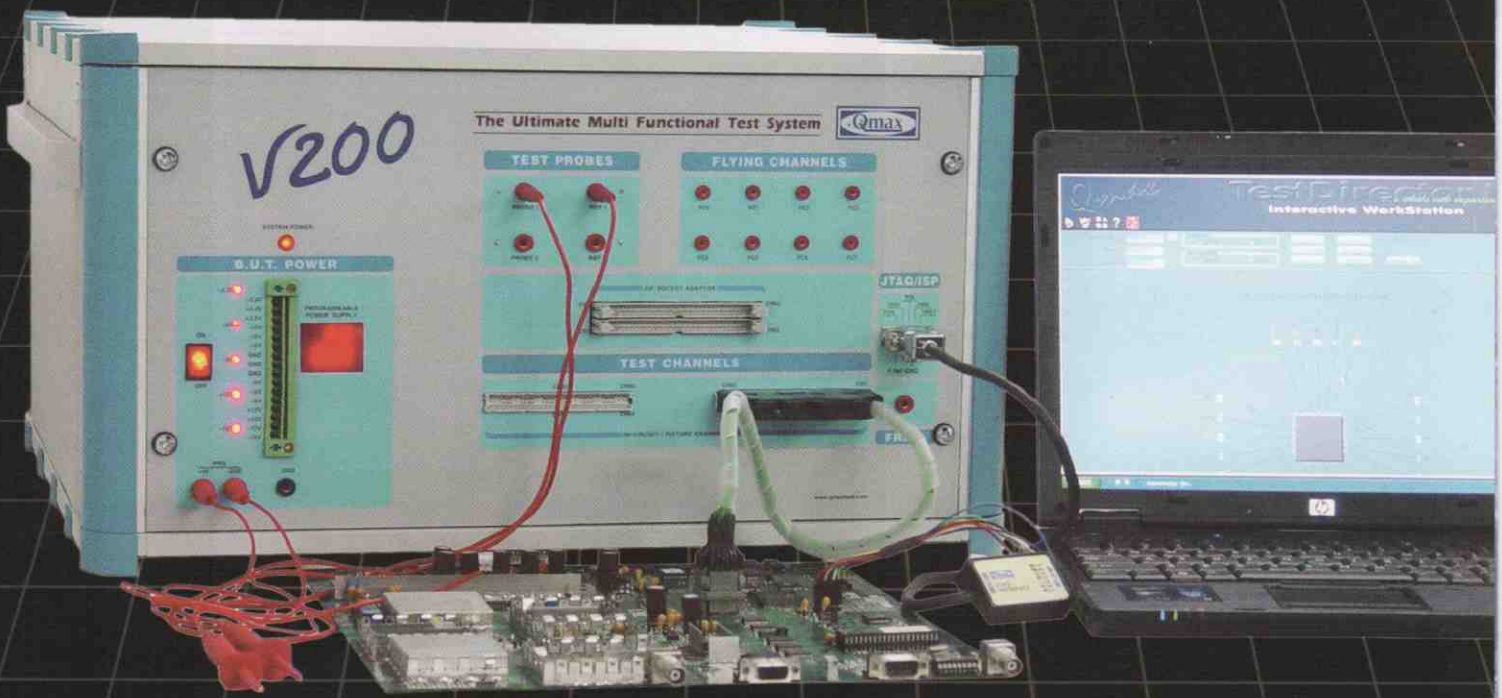
V200
DESK-TOP ATE



Unique Features

- VHDL based Device Library
- Card Edge Functional Test
- Guided Probe back-tracking
- Integrated Boundary Scan Controller
- Fault Simulation
- Fault Dictionary
- Programmable Time base in 2048 steps
- User defined analog stimulus QSM VI
- PythonTD Test language

Qmax

Qmax V200, a tester for past, present & future PCBs / Devices and Modules

V200 is a cost effective mini ATE system, designed to cater the needs of PCB test and repair depots, keeping in mind the changing PCB technology and the challenges in testing them off-line. It can provide complete PCB test and diagnostic functions for any kind of PCB including the latest very high density complex PCBs with high pin count PQFP, FPGA VLSI chips.

It is a Combinational – Mixed Signal Test System with the addition of Integrated Boundary Scan Test for the latest generation chips. It has Card Edge Functional Test for both digital and analog, and In-Circuit Functional Test for localized test of individual devices including LSI / VLSI / Memory and Microprocessors. It also incorporates an advanced QSM VI with auto "Best Fit Curve" Algoritm.

Features of V200 Hardware:

V200 is designed as a Combinational Tester with Digital /Analog and Mixed Signal Test capabilities through simple clips and probes or through card edge or as a cluster tester with a special test fixture for up to 256 test pins. In addition, it has the Boundary Scan Test option for virtual pin test where the number of virtual test pins has no physical limit. Its basic timing unit is 100ns and thus can generate test patterns at 10 MHz data rate. The timing units are programmable in 2048 steps from 100ns to 200µs, (100ns, 200ns, 300ns etc up to 200 µs) thus allowing accurate pattern timings. It has 8K x 4 RAM behind each digital pin electronics and 8K x 24 RAM behind each analog channel. Its advanced sequencer allows external event synchronization or handshake, which are very essential in complex microprocessor tests.

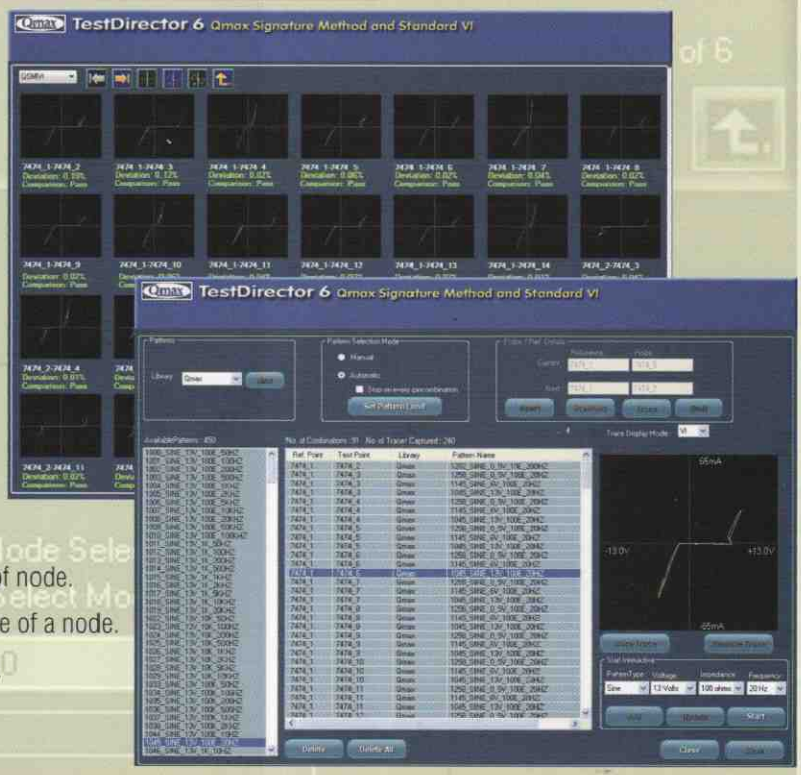
TD6 Interactive WorkStation

In-Circuit Functional Test at its Best

- Functional Test facility for testing individual ICs in In-Circuit or Out-of-Circuit.
- Pin Status Check & In-built DRC (Design Rule Checker).
- IEEE Standard VHDL language in behavioral description of the function of the chip in its library.
- Device programming for SSI / MSI in Qmax Device Development Language (QDDL)
- PythonTD Test language for Analog / Mixed signal device stimulus and output evaluation.
- Auto compensation is extended for all digital devices (not limiting to SSI /MSI) and thus LSI / VLSI chips can be tested in its In-Circuit configuration without the need to learn from a known good board.
- Unified Library of 31K+ devices and device test comprehensives report for validation of Library Test programs developed by a user.
- Identify "Unknown" devices using advanced foot print match algorithm and covers SSI / MSI / LSI devices.

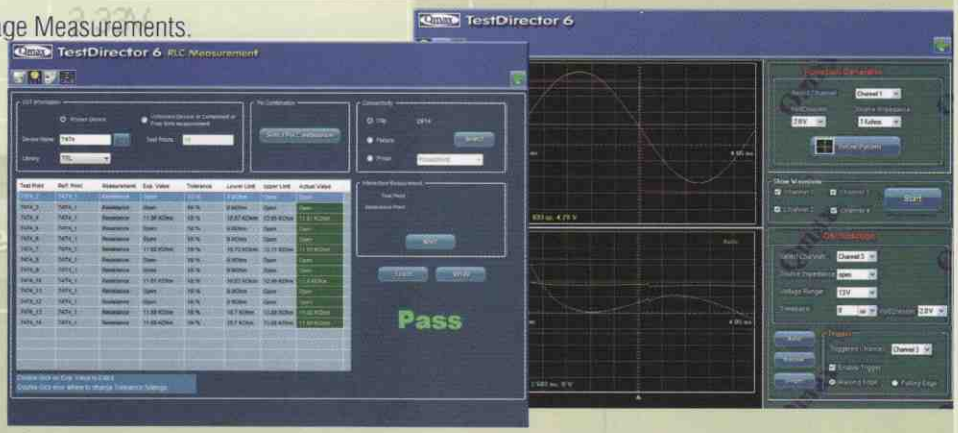
User defined QSM VI Stimulus

- Standard and user defined wave pattern as stimulus for VI Trace and thus not limiting the VI trace to simple sine wave alone.
- User defined wave pattern can be any mathematical wave shape such as sine / triangle / square / step /ramp or even arbitrary patterns as desired by user and can be stored in the Library for possible re-use.
- The frequency is fully programmable from as fast as 100 KHz as a result of ***V200***'s vast time base selection capability.
- "Best Fit Curve" — an unique feature, where the best drive pattern is automatically suggested to the user for the characteristics of the UUT to increase the fault coverage.
- Advanced alogrithm suggests the failing pin within a device with % probability.
- Use of Step wave is useful in analyzing transient response of node.
- Frequency Sweep generation to trace the frequency response of a node.
- Incorporates interactive mode as well as learn and compare.
- Fixed Reference, any pin to any pin or user combination.
- Learn net-list from the clip status links option.



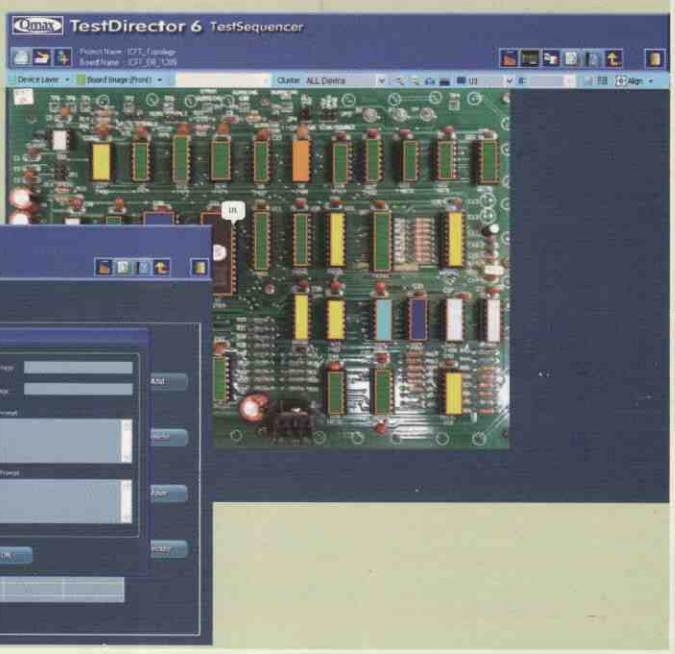
Measurement Functions & Other Utilities

- Resistance / Inductance / Capacitance / Voltage Measurements.
- Diode Measurements.
- Frequency Measurement.
- 3 Channel - 10 Mega Sample Scope with Programmable Load.
- 3 Channel Function Generator.



TD6 TestSequencer

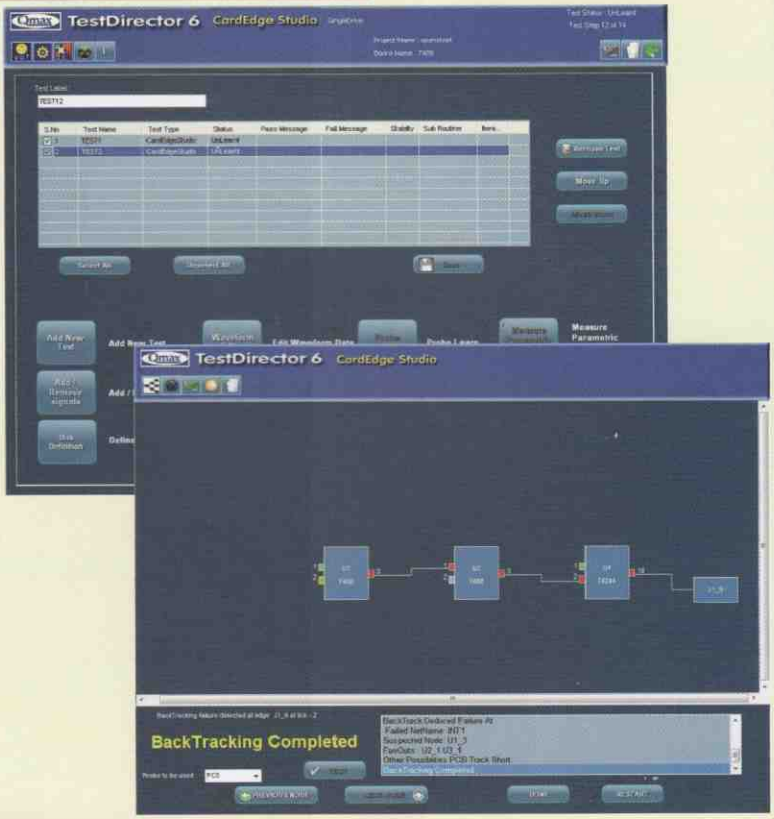
- For Sequencing of multiple tests with conditional branching, messaging, user prompting, external trigger and external handshake.
- Board level test using combination of isolated device test (ICFT), QSM VI, Measurements, Card Edge Functional Test, Integrated Card Edge + Boundary Scan Test*, all in one test program.
- Full graphical TPS development using JPEG image of the PCB under test, tagging devices and pins.
- Adding tests to the devices, cluster with just a right click of the mouse. Learn, verify and test options using mouse click on the device location.



* *Boundary Scan Software need to be purchased for enabling this facility.*

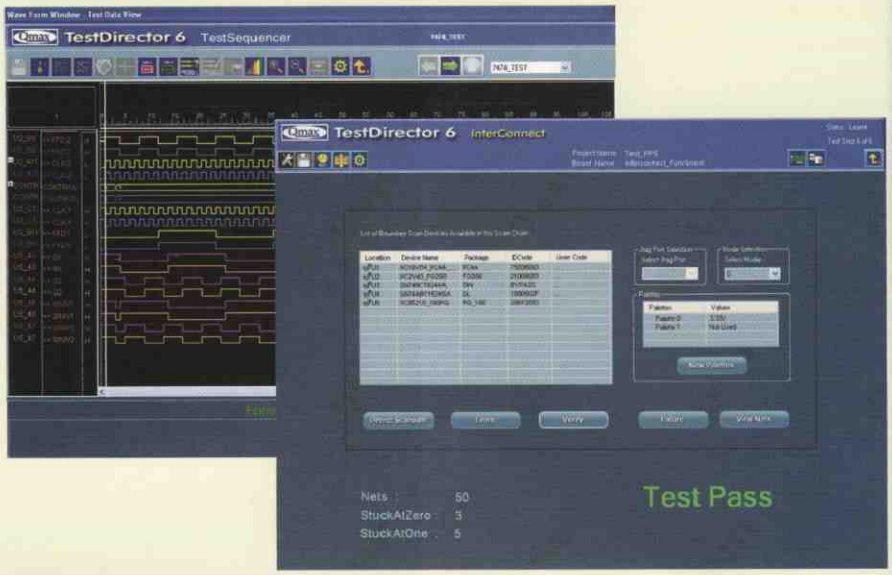
Card Edge Functional Test at its Best

- User can develop test program for complex boards with ASICs and BGAs, where no functional data are available.
- User can generate the test vectors using the graphical waveform editor or PythonTD test vector generator, where the primary I/O pins can be either physical edge pin / In-Circuit pin or a JTAG Virtual Boundary Scan Pin.
- User can either learn the expected output from a known good board or define the expected output using graphical waveform editor or simulate the expected output using VHDL Simulation or the PythonTD test language with mask / tolerance editing facilities.
- Automatic Guided Probe Back Tracking for Fault Isolation up to node level.
- Graphical waveform editor and PythonTD supports Digital / Analog and Mixed Signal I/Os.
- The Test program developed can be used for a device / cluster or a complete PCB.
- In case of cluster or whole board, user needs to input the netlist of the circuit, assign input /output pins for tester channel for automatic generation of guided probe back tracking of internal nodes.



Boundary Scan Test Software *(Optional)*

- Boundary Scan uses simple 5-wire connector (J-TAG) to interface to the PCB under test, eliminating the need for test pin contact (Virtual Test Pin Test Concept).
- Using Boundary Scan Software package and vendor supplied BSD Files, ID Code Read, User Code Read, Integrity Test and Interconnect Test can be performed.
- Learn and compare option for interconnect test, where no netlist is available.
- Functional Test for BS devices and Non-Boundary Scan Devices.
- Integrated Card Edge and Boundary Scan Test for Interconnect Test and Board Functional Test.



TD6 TestStation

- Programs developed in TestDirector6 TestSequencer can be exported to TestStation
- Test only function and no program /data /tolerance can be modified.
- Auto run mode, Manual run mode with options for stop on first failure, details on failure and graphical mode of testing.
- User defined Error Log reporting, Failure analysis, statistics and data log.
- Optional Remote Monitoring of yield and statistics.

SPECIFICATIONS

SYSTEM

Test Points	Up to 96 Digital In-Circuit Testing (16 Ch. per card)
	Up to 256 Analog Signature Testing
	Un-limited Virtual Test Points
Pattern Rate	10 MHz -Digital testing (Max.),
	10 MHz -Analogue testing, (20 MHz sampling rate)
	100 KHz – QSM VI
Time Base	Programmable from 100ns to 200µs in steps of 100ns (2048 steps)
Dynamic Guarding	Up to 8 channels, allocated automatically. Additionally, any digital channels can be used for Guarding applications.

DRIVERS / SENSORS

DIGITAL

Driver/Sensor card	16 channels bi-directional RAM based channel per card up to 96 max
Drive Level & Resolution	±10V programmable in 80 mV steps
Sense Level & Resolution	±10V programmable in 40 mV steps
Current	650 mA sink & source limit as per Interim Defence Standards 00-53/1.
Driver state	Hi, Low and Tri-state

ANALOG

No. of Channels	3, expandable up to 6, each 12 bit DAC / ADC RAM based.
Analog Multiplexer	Switchable to any test channel available.
Driver output current	250mA per channel.
Drive Pattern	User definable and standard waveform
Drive Source Impedance	Programmable in 5 steps
Drive current/voltage	± 250mA maximum / ±13 volt per Channel.

IN-CIRCUIT TEST

Digital	Clip on test using systems device library and simulator output.
Analog	Clip on test using systems device library and calculated output.
Simulator	Industry grade VHDL / QDDL / PythonTD Simulators.

OTHER FEATURES

Size of test	8K-deep test vectors in single burst mode. Unlimited vector depth in interactive hand shake mode.
Analog Measurements	R, L, C, V and F
	Res.: 10 Ohms to 1MOhms **Cap.**: 200pF to 10000µF **Inductance:** 100µH to 10H **Voltage:** +/- 13V **Frequency:** Up to 48 MHz Three Channel Oscilloscope with programmable load.
BUT Powersupply	+3.3V@10A / +5V@10A / –5V@10A / +12V@8A / –12V@8A. *Optional* : Programmable Powersupply (0-36V @ 6A) up to 2 Nos.

SYSTEM GENERAL SPECIFICATIONS

Power Requirement	230V / 5A or 110V AC / 10A, 1200W, 50-60Hz
Physical Dimension	560mm (w) X 540mm (d) X 310mm (h), Rittal, Ri Case 6U Cabinet
Weight	30 Kg (net)

TEST SOFTWARE

TD6 Interactive WorkStation	Standard
TD6 TestSequencer	Standard
TD6 TestStation	Standard
CircuitTracer for Reverse engineering	Optional
Edwin for schematic generation	Optional
Boundary Scanning S/W	Optional
Russian Device Library	Optional

GENERAL *(Recommended)*

Controller	Core2-Duo or latest
Operating System	Windows XP Professional SP2 / Vista Business Edn. / Windows 7 Professional Edn.
RAM	Minimum 2 GB
Hard Disk	80 GB with 2 partition
Interface	USB 2.0 (min. of 4 USB ports)
User Control	keyboard / Mouse / Optional – Foot switch / external trigger.
Test Interface	Clips – Probes / Card edge / customized test fixtures / J-TAG

TEST INTERFACE

IN-CIRCUIT WALKING CLIPS

DIP Clips –Top access	8-64 pins
DIP Clips – Bottom	8-40 pins
PLCC – Clips	up to 84 pins
SOIC – Clips	up to 28 pins
QFP – Clips	On request
TO5 package	
TO9 package	
Russian Device Clips	up to 40 pins
JTAG	5 wire simple connector for boundary scan tests.

OUT-CIRCUIT

DIP 40 & 64

SMDs – SOP / TSOP / PQFP / SOIC / SOJ / PLCC / Russian up to 64 pins

CUSTOMISED

Card edge / Bed of nails

Qmax

— where standards are set; not matched.

For more information mail to:
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