QT200nxT

NEXT GENERATION MIXED SIGNAL TEST SYSTEM

QT200nxT is a cost effective Next Generation Mixed Signal Functional Test System, designed to cater the needs of PCB test and repair depots, keeping in mind the changing PCB technology & the challenges in testing them off-line. It can provide complete PCB test and diagnostic functions for any kind of PCB including the latest very high density complex PCBs with high pin count PQFP, FPGA, VLSI chips.

It is a combinational-Mixed Signal Test System with the addition of Integrated Boundary Scan Test for the latest generation chips. It has Card Edge Functional Test for both digital & analog & In-Circuit Functional Test for localized test of individual devices including LSI / VLSI / Memory & Microprocessors. It also incorporates an advanced QSM VI with auto "Best Fit Curve" Algorithm. The in-built computer & the monitor makes it a perfect portable system.

QT200nxT OVERVIEW

- 48 Channels expandable up to 96
- Digital, Analogue & Mixed Signal Test Capability
- Unlimited Virtual Test Pins
- Boundary Scan Test enabled
- Vast device library
- Best Fit Curve feature to enhance fault coverage
- In-built computer with Core-i3 processor, 4 GB RAM, 500 GB HDD
- In-built 12" industrial monitor

QT200nxT is designed as a Combination Tester with Digital, Analog and Mixed Signal Test capabilities through simple clips and probes or through card edge or as a cluster tester with a special test fixture for up to 256 test pins (Basic system comes with 48 channels). In addition, it has the Boundary Scan Test option for Virtual pin test where the number of Virtual test pins has no physical limit.

Its basic timing unit is 100ns and thus can generate test patterns at 10MHz data rate. The timing units are programmable in 2048 steps allowing accurate pattern timings. Its advanced sequencer allows external event synchronization or hand-shake, which are essential in complex microprocessor tests.

QT200nxT SOFTWARE FEATURES

IN-CIRCUIT FUNCTIONAL TEST

- » Functional Test facility for testing individual ICs in In-Circuit or Out-of-Circuit.
- » Pin Status Check & In-built DRC (Design Rule Checker).
- » IEEE Standard VHDL language in behavioral description of the function of the chip in its library.
- » Device programming for SSI / MSI in Qmax Device Description Language (QDDL).
- » PythonTD Test language for Analog / Mixed signal device stimulus and output evaluation.
- » Auto compensation is extended for all digital devices (not limiting to SSI / MSI) and thus LSI / VLSI chips can be tested in its In-Circuit configuration without the need to learn from a known good board.
- » Unified Library of 33K+ devices & devices test comprehensives report for validation of Library Test programs developed by a user.
- » Identify “Unknown” devices using advanced foot print match algorithm & covers SSI / MSI / LSI devices.

USER DEFINED QSM VI STIMULUS

- » Standard and user defined wave pattern as stimulus for VI Trace and thus not limiting the VI trace to simple sine wave alone.
- » User defined wave pattern can be any mathematical wave shape such as sine / triangle / square / step / ramp or even arbitrary patterns as desired by user & can be stored in the Library for possible re-use.
- » The frequency is fully programmable from as fast as 100KHz as a result of **QT200nxT**'s vast time base selection capability.
- » “Best Fit Curve”- an unique feature, where the best drive pattern is automatically suggested to the user for the characteristics of the UUT to increase the fault coverage.
- » Advanced algorithms suggests the failing pin within a device with % probability.
- » Use of Step wave is useful in analyzing transient response of node.
- » Frequency Sweep generation to trace the frequency response of a node.
- » Incorporates interactive mode as well as learn & compare.
- » Fixed Reference, any pin to any pin or user combination.
- » Learn net-list from the clip status links option.

MEASUREMENT FUNCTIONS & OTHER UTILITIES

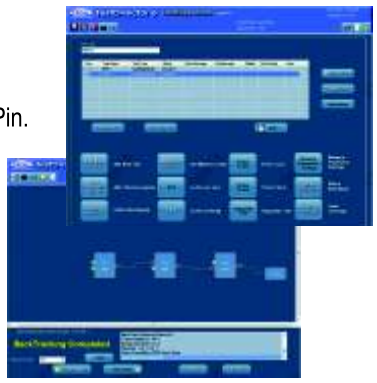
- » Resistance / Inductance / Capacitance / Voltage Measurements.
- » Diode Measurements.
- » Frequency Measurements.
- » 3 Channel-Digital Oscilloscope with Programmable Load.
- » 3 Channel Function Generator.

TESTSEQUENCER

- » For Sequencing of multiple tests with conditional branching, messaging, user prompting, external trigger & external handshake.
- » Board level test using combinational of isolated device test (ICFT), QSM VI, Measurements, Card Edge Functional Test, Integrated Card Edge + Boundary Scan Test* all in one test program.
- » FII graphical TPS development using JPEG image of the PCB under test, tagging devices & pins.
- » Adding tests to the devices cluster with just a right click of the mouse. Learn, verify and test options using mouse click on the device location.

** Boundary Scan Software need to be purchased for enabling this facility.*

CARD EDGE FUNCTIONAL TEST

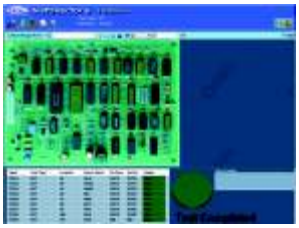


- User can develop test program for complex boards with ASICs and BGAs, where no functional data are available.
- User can generate the test vectors using the graphical waveform editor or Python TD test vector generator, where the primary I/O pins can be either physical edge pin/In-Circuit pin or a JTAG Virtual Boundary Scan Pin.
- User can either learn the expected output from a known good board or define the expected output using graphical waveform editor or simulate the expected output using VHDL Simulation or the Python TD test language with mask/tolerance editing facilities.
- Automatic Guided Probe Back Tracking for fault isolation up to node level.
- Graphical waveform editor and Python TD supports Digital/Analog and Mixed Signal I/Os.
- The Test program developed can be used for a device/cluster or a complete PCB.
- In case of cluster or whole board, user needs to input the netlist of the circuit, assign input/output pins for tester channel for automatic generation of guided probe back tracking of internal nodes.

BOUNDARY SCAN TEST *(Optional)*

- The system meets IEEE 1149.1 & IEEE 1532 standards.
- Boundary Scan uses simple 5-wire connector (J-TAG) to interface to the PCB under test, eliminating the need for test pin contact (Virtual Test Pin Test Concept).
- Using Boundary Scan Software package and vendor supplied BSD Files, ID Code Read, User Code Read, Integrity Test and Interconnect Test can be performed.
- Learn and compare option for interconnect test, where no netlist is available.
- Functional Test for BS devices and Non-Boundary Scan Devices.
- Integrated Card Edge and Boundary Scan Test for Interconnect Test and Board Functional Test.

TESTSTATION



- Programs developed in TestDirector6 TestSequencer can be exported to TestStation.
- Test only function and no program / data / tolerance can be modified.
- Auto run mode / Manual run mode with options for stop on first failure, details on failure and graphical mode of testing.
- User defined Error Log reporting, Failure analysis, statistics and data log.
- Optional Remote Monitoring of Yield and statistics.

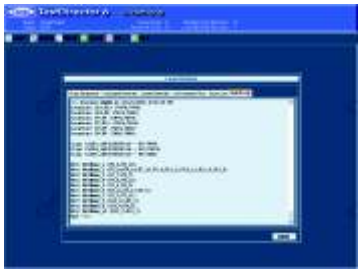
BOARD LEVEL SIMULATION & FAULT COVERAGE

- Off-Line Simulation helps develop TPS without tying up the ATE system.
- Advanced On-Line Simulation support for increased fault coverage for boards that fail to initialize.
- Fault Simulation Software for Board Test Program validation and test comprehensiveness.
- Fault coverage report.

INTEGRATED DEVICE TEST ENVIRONMENT – IDTE *(Optional)*

- For developing new Digital Device Models in the library using VHDL / QDDL Language behavior.
- For developing new Analog/Mixed signal device models using Python TD Test Language and adding it in the Library.
- Graphical Test Program Generation Feature.

CIRCUIT TRACER *(Optional)*



- Using multiple clips, Edge connectors / Probes and JTAG I/O pins, the connectivity between devices can be learnt and a netlist created.
- Created net list can be imported into optional Edwin CAD package for schematic generation.

QT200nxT HARDWARE FEATURES

MAIN SEQUENCER / CONTROLLER :

- System based on highly programmable dedicated test vector processor.
- USB 2.0 Interface between the main sequencer and user PC.
- The system has 1K X 60 Bit RAM for instruction register.
- Up to 1024 test sequences can be preprogrammed to run automatically with option of unconditional looping up to 32K cycles.
- Sequencer operating speed up to 100 MHz.
- Basic timing unit programmable from 100ns to 655µs in steps of 100ns
- Time duration is programmable up to 256.
- Test vector depth up to 256K.

DIGITAL MODULE (Programmable Palette):

- Minimum of 48 Channels expandable up to 96 in steps of 16.
- Maximum skew rate between two channels is ±10 nS.
- Digital drive speed up to 10 MHz.
- Slew rate up to 600V/microsecond.
- Data rate programmable from 100 ns to 160 ms in steps of 100ns.
- Drive level up to +12V / –12V programmable, 40mV steps.
- Sense level up to +12V / –12V programmable, 40 mV steps.
- Memory behind each pin 256K X 4.
- Dynamic current capacity of pin driver is ±650mA.
- Pin driver is capable of driving all three states of Hi, Low & Tri-State.
- Every digital channel has 2.2KE of internal Pull up/ Pull down and its software programmable.
- Two different palette setting for digital Drive / Sensing.
- Flying channels (sharing) up to 8 No.s for guarding purpose.

ANALOG MODULE:

Analog module can be used for mixed signal and analog test. Four independent analog channels can be multiplexed to any of the 256 test channels + 8 flying channels.

- Analog channels are multiplexable to all 256 test channels.
- Maximum of 6 channels.
- Analog sampling rate is 25 MHz.
- Generates output frequency up to 100 KHz.
- Memory behind each pin 256 K X 28 (Drive & Receive)
- Module has 4 different programmable voltage ranges as ±1V, ±3V, ±6V, ±13V & ±24V (Optional)
- Drive current maximum up to ±100 mA / per channel at maximum voltage range.
- Drive pattern Sine/Triangular/Rectangle/Ramp/DC & user definable.
- Selectable 10 source impedances are 10E, 50E, 100E, 500E, 1KE, 5KE, 10KE, 50KE, 100KE, 500KE and Open.
- 14 bit resolution of DAC / ADC to provide very accurate results.

ANALOG CARD as VI SIGNATURE MODULE (QSM):

- Drive voltage from 0.5 to 13V & 24V (optional).
- Available drive patterns are Sine, Square, Tri-angular, Ramp, DC and user definable.
- Source impedances are from 10 Ohms to 500 KOhms.
- VI test frequency from DC to 100 KHz.
- No of channels available basic is 96 and expandable up to 256 max.
- Drive pattern length is user programmable up to 256 K samples.
- Fully user programmable VI traces drive patterns.
- User test probes up to 2 pairs for interactive testing purpose.

AC – PMU MODULE (Only Freq. Measurement):

- Frequency measurement up to 50 MHz (@0.1% accuracy) through front panel socket.

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BOUNDARY SCAN (Test Technique Module):

Built in Integrated J-TAG port on the front panel of equipment along with Digital Channels for Boundary Scan Testing and coverage of Non Boundary Scan Devices through Virtual Test pins (BS pins) and ATE Digital channels.

- Basic Single Chain.
- Compatible with IEEE Standards.
- Nominal J-TAG Clock frequency is 1 MHz and it can be programmable up to maximum of 10 MHz.
- 128 Kbits RAM based Drive / Sense.

UUT Power Supply:

Fixed SMPS power supplies are integrated for UUT testing.
System has 5 Fixed Volt in Volt / Current ranges of +3.3V@10A, +5V@10A, –5V@10A, +12V@6A, –12V@6A.

Hardware Health Check Tools:

Apart from main application software, the system supplied with Test Jigs applications to do the Health Check of system.
Test Jig application has following facilities:

- Automated self test facility for all hardware modules.
- Manual test facility for diagnostic the failure and re-servicing the hardware module.
- Auto calibration software module for calibrating analog channels and digital channels.
- Measurement tool kit for auto calibration is optional.

Controller & General System Specifications:

Computer	: In-built Computer – Core-i3 Processor, 4 GB RAM, 500 GB HDD, 4-USB Slots
Built-in Monitor	: Standard industrial 12" Monitor
System Power	: Single Φ AC 110V-60Hz / 230V-50Hz (Max. 1 KVA)
Operating Temp.	: 35°C ± 3°C
Dimensions	: 6U Schroff Cabinet 470(W) X 415(D) X 290(H).
Weight	: Approx. 30 Kgs.

Test Interface

In-Circuit Walking Clips
DIP Clips – Top access & Bottom access
PLCC Clips
SOIC Clips
QFP Clips
TO5 Package
TO9 Package
Russian Device Clips
J-TAG – 5 wire simple connector for Boundary Scan tests

Out-Circuit
DIP 40 & 64
SMD - SOP/TSOP/PQFP/SOIC/SOJ/PLCC/Russian up to 64 pins

Customised
Card edge / Bed of Nails / Automated XYZ Prober (Optional)
(For details of Standard / Optional accessories contact Qmax representatives)